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APPLICATION FOR U.S. LETTERS PATENT

Title:

LOW INJECTION CHARGE PUMP

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LOW INJECTION CHARGE PUMP

The present invention relates to charge pumps which have particular utility in phase lock loop (PLL) and delay lock loop (DLL) circuits.

DISCUSSION OF THE RELATED ART

Phase lock loop and delay lock loop circuits are widely used for frequency multiplication and to produce precise delay signals from an incoming clock signal. When such circuits are used in high speed environments such as serial communications, they often need very low phase offset between input and output signals. One common PLL architecture is shown in Figure 1 and is described in greater detail in the article "A Wide-Bandwidth Low-Voltage PLL for Power PC™ Microprocessors" by Alvarez et al., Journal of Solid-State Circuits, Vol. 30, No. 4 April 1995. The entire contents of this article are incorporated herein by reference. The PLL of Figure 1 relies on a charge pump 11 which receives UP 15 and DOWN 17 pulse signals from a phase detector 13 with the output of the charge pump 11 feeding a PLL loop integrating

filter 19. The filter 19 drives a voltage controlled oscillator 20 and the output of oscillator 20 is frequency divided by programmable divider 22. The output of frequency divider 22 drives a delay equalization circuit 24 and different taps of the delay equalization circuit are provided to respective clock regenerator circuits 26, one of which is fed to a programmable divider which in turn feeds one of the inputs of phase detector 13. A system clock SYSCLK signal is applied to the other input of phase detector 13 through a programmable delay match circuit 30. With this circuit, the regenerated clock signals RCLK are frequency and phase locked to the SYSCLK signal. Further details of the operation of the Figure 1 circuit can be found in the noted Alvarez et al. article.

One problem with charge pump 11 is that with real world transistor devices and process spreads, when the PLL is in lock, neither the UP 15 nor the DOWN 17 pulses occur. This causes a dead-band in the PLL response where differences in phase between an applied system clock signal SYCLK and a PLL generated clock signal CPU cannot be detected. The usual remedy for such a situation is to make sure the UP 15 and DOWN 17 pulses occur under all conditions of operation, that is

the duration of the up and down pulses may be limited to very short durations, but they never disappear completely. However, there is a problem in producing a very short pulse at the output of charge pump 11, as it requires a very fast turn on and turn off of the charge pump 11 without a large amount of charge coupling which might distort the output signal.

Figure 2 illustrates one possible CMOS implementation of a fast switching charge pump 21 which produces a fast current spike at its output 23. Current sources 25 and 27 are switched by respectively serially connected p-channel and n-channel transistors 29, 31 in response to respective $\overline{\text{DOWN}}$ (the inverse of a DOWN pulse) and UP pulses applied to respective gates 33 and 35.

The operation of the Figure 2 circuit is represented by the waveform produced by the Figure 2 circuit in response to a UP input pulse, which is shown in Figure 5. As seen, the output current upon the turn-off of transistor 31 goes positive in the shaded region of the output signal before returning to a steady zero state. This output current overshoot is caused by the considerable capacitive charge coupling 41

which occurs between the gate and output of transistor 31. A similar situation exists when transistor 29 is switched by the DOWN pulse due to capacitive charge coupling 43 between the gate and output of transistor 29. Any mismatch in the charge coupling at transistors 29 and 31 causes current pulse distortion which is applied to the VC0. The unbalanced charge coupling is compensated by a phase offset at the input to the phase detector 13. Thus, the loop must adjust the UP/DOWN pulse lengths to ensure the net charge flow is zero. It would be desirable to minimize this current pulse distortion.

Figure 3 illustrates a CMOS charge pump 41 which does not suffer from capacitive charge coupling due to the presence of p-channel and n-channel biasing transistors 43, 45. The transistors 43, 45 are DC biased so that they pass the correct amount of current during switching operations of transistors 29 and 31. Although the Figure 3 arrangement significantly mitigates the problem of current pulse distortion inherent in the Figure 2 circuit, operation of the Figure 3 circuit is relatively slow, as shown in Figure 6, which illustrates in cross-hatching a trailing edge of the output pulse current produced in response to an UP pulse at the gate

of transistor 31. The illustrated slowness in transistor turn-off is attributed to a parasitic load capacitor 57 which exits across the UP source and drain of the UP switching transistor 31. A similar parasitic load capacitor 53 is present across the source and drain of transistor 29. The parasitic load capacitors 51 and 53 produce slow turn off of transistors 29 and 31 and a delay in the trailing edge of the output signal, which is again applied as a phase offset at the input to the phase camparator.

What is needed is a charge pump for use in a PLL and DLL which is fast and which mitigates problems with current overshoot and transistor turn-off slowness.

SUMMARY OF THE INVENTION

The present invention provides a charge pump which has a fast switching characteristic and which mitigates the effected noise, current overshoot and transistor turn-off slowness at the charge pump output. The invention also provides a PLL or DLL circuit which uses the charge pump.

The charge pump incorporates n-channel and p-channel switching transistors and n-channel and p-channel biasing transistors, as well as a capacitive coupling of complementary versions of the signals used to switch the n-channel and p-channel switching transistors to respective nodes which interconnect the p-channel switching and biasing transistors and the n-channel switching and biasing transistors. The capacitively coupled complementary signals cause the charge pump to maintain a fast switching response without output waveform distortion.

These and other features and advantages of the invention will be more clearly understood from the following detailed description of the invention which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a conventional phase lock loop (PLL) circuit which employs a charge pump 11;

Figure 2 illustrates a charge pump circuit which may be used in the PLL of Figure 1;

Figure 3 illustrates a charge pump circuit which is an improvement upon that illustrated in Figure 2;

Figure 4 illustrates a charge pump circuit in accordance with an embodiment of the invention;

Figure 5 illustrates a timing diagram which shows operation of the charge pump illustrated in Figure 2;

Figure 6 illustrates a timing diagram of the operation of the charge pump depicted in Figure 3;

Figure 7 illustrates the timing diagram of the charge pump of Figure 4 in accordance with an exemplary embodiment of the invention; and

Figure 8 illustrates a processor system which may employ the charge pump of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 4 illustrates an exemplary embodiment of a CMOS charge pump 61 in accordance with the invention. The circuit is essentially the same as that illustrated in Figure 3, except for the addition of coupling capacitors 65 and 69 which respectively receive an inverted form of the $\overline{\text{DOWN}}$ signal applied to gate 33, that is a DOWN signal, and capacitor 69 which receives an inverted form of the UP signal, that is an $\overline{\text{UP}}$ signal.

The signal DOWN is applied through capacitor 65 to the common node A of respective switching and D.C. biasing transistors 29 and 43, while the switching signal $\overline{\text{UP}}$ is applied through capacitor 69 to the common node 13 between respective transistors 45 and 31. The provision of the switching signals DOWN and UP to respective nodes A and B provides a fast turn on and turn off of the transistors 29 and 31 without waveform distortion in the resulting output signal. The voltage on the capacitors 65 and 69 settles to a DC point where the voltage across transistors 29 and 31 is minimal, but the net effect is a fast turn on and

turn off of transistors 29 and 31 with low capacitively coupled charge injection.

Figure 7 illustrates the output of the Figure 4 circuit when an UP pulse is applied. As shown, the output current switches very quickly following the switching timing of the UP pulse. As also shown, there is no significant waveform distortion in the output signal which might produce a phase offset at the phase comparator 13 of a PLL or DLL.

The charge pump 61 of the invention can be used in the Figure 1 phase lock loop circuit, as well as in delay lock loop (DLL) circuits to achieve fast turn on and turn off in response to short duration pump UP and pump DOWN input signals which may be generated in the PLL or DLL to keep it operating, even when phase lock is achieved.

The charge pump 61 may also be used in any situation where fast switching of logic signals is needed, including in high speed processor systems. As shown in Figure 8, a processor system, such as a computer system, for example, generally comprises a central processing unit (CPU) 210, for example, a microprocessor, that communicates with one or more

input/output (I/O) devices 240, 250 over a bus 270. The computer system 200 also includes random access memory (RAM) 260, a read only memory (ROM) 280 and may also include peripheral devices such as a floppy disk drive 220 and a compact disk (CD) ROM drive 230 which also communicate with CPU 210 over the bus 270. Any one or more of the elements depicted in Figure 8 may use the charge pump 61 of the invention and/or a PLL or DLL which employs the inventive charge pump 61.

While an exemplary embodiment of the invention has been described and illustrated, it should be apparent that many modifications and substitutions can be made without departing from the spirit and scope of the invention. Accordingly, the invention is not limited by the foregoing description, but is only limited by the scope of the appended claims.